

The background of the slide is a dark blue field filled with numerous curved, parallel lines in various colors including yellow, cyan, magenta, and light blue. These lines are arranged in a pattern that suggests a sense of motion or a digital interface.

# ***8255 A PROGRAMMABLE Peripheral INTERFACE***

# INTRODUCTION

**8255** is a popularly used parallel, programmable input-output device. It can be used to transfer data under various conditions from simple input-output to interrupt input-output. This is economical, functional, flexible but is a little complex and general purpose i/o device that can be used with almost any microprocessor.

# PORTS OF 8255A

## Ports of 8255A

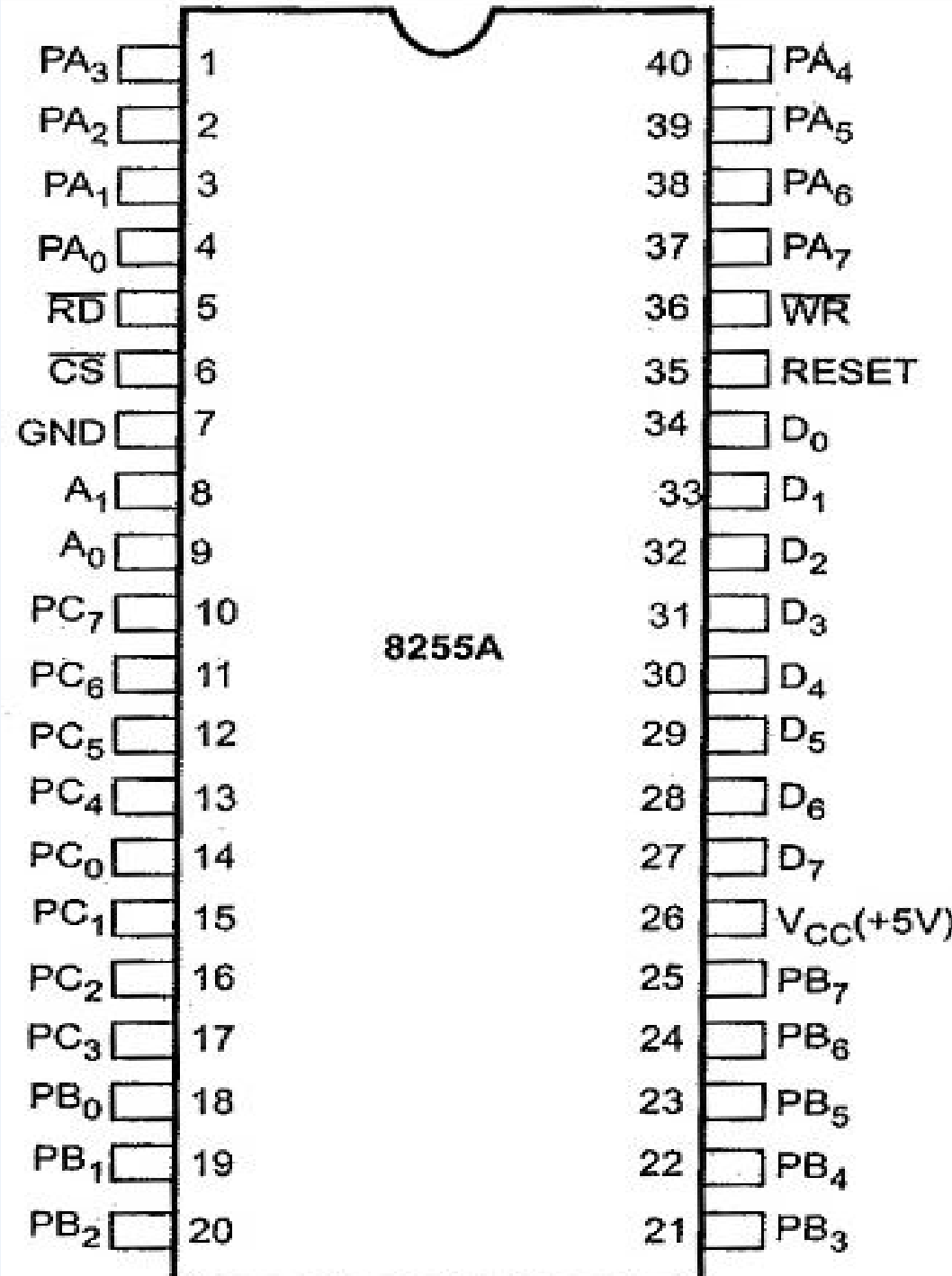
8255A has three ports, i.e., PORT A, PORT B, and PORT C.

- **Port A** contains one 8-bit output latch/buffer and one 8-bit input buffer.
- **Port B** is similar to PORT A.
- **Port C** can be split into two parts, i.e. PORT C lower (PC0-PC3) and PORT C upper (PC7-PC4) by the control word.

These three ports are further divided into two groups, i.e. Group A includes PORT A and upper PORT C. Group B includes PORT B and lower PORT C. These two groups can be programmed in three different modes, i.e. the first mode is named as mode 0, the second mode is named as Mode 1 and the third mode is named as Mode 2.

# PIN DIAGRAM

- PA0 - PA7 - Pins of port A
- PB0 - PB7 - Pins of port B
- PC0 - PC7 - Pins of port C
- D0 - D7 - Data pins for the transfer of data
- RESET - Reset input
- RD' - Read input
- WR' - Write input
- CS' - Chip select
- A1 and A0 - Address pins



| Pin name | No.of pins | I/O             | functions   |
|----------|------------|-----------------|---|
| PA0-PA7  | 8          | i/o<br>Tristate | ➤ Port can be configured either input or output by software   |
| PB0-PB7  | 8          | i/o<br>Tristate | ➤ Port has output latch buffer and input buffer<br>➤ PA can be programmed by mode 0 , mode 1, mode 2 .  |
| PC0-PC7  | 8          | i/o<br>Tristate | ➤ PB can be programmed by mode 0 and mode 1.<br>➤ PC can be programmed by bit set/reset operation.<br>➤ Port C can be divided into two 4 bit ports namely PC7-PC4 & PC3-PC0 and used for control signals to PA and PB |
| D0-D7    | 8          | i/o<br>Tristate | ➤ Used for data transfer with MPU<br>➤ Transfer of control words to PPI<br>➤ Read status information from PPI   |

# WR


It stands for write. This control signal enables the write operation. When this signal goes low, the microprocessor writes into a selected I/O port or control register.

# RESET

This is an active high signal. It clears the control register and sets all ports in the input mode.

# RD

It stands for Read. This control signal enables the Read operation. When the signal is low, the microprocessor reads the data from the selected I/O port of the 8255.



# CS

It stands for Chip Select. A LOW on this input selects the chip and enables the communication between the 8255A and the CPU. It is connected to the decoded address, and  $A_0$  &  $A_1$  are connected to the microprocessor address lines.

Their result depends on the following conditions –

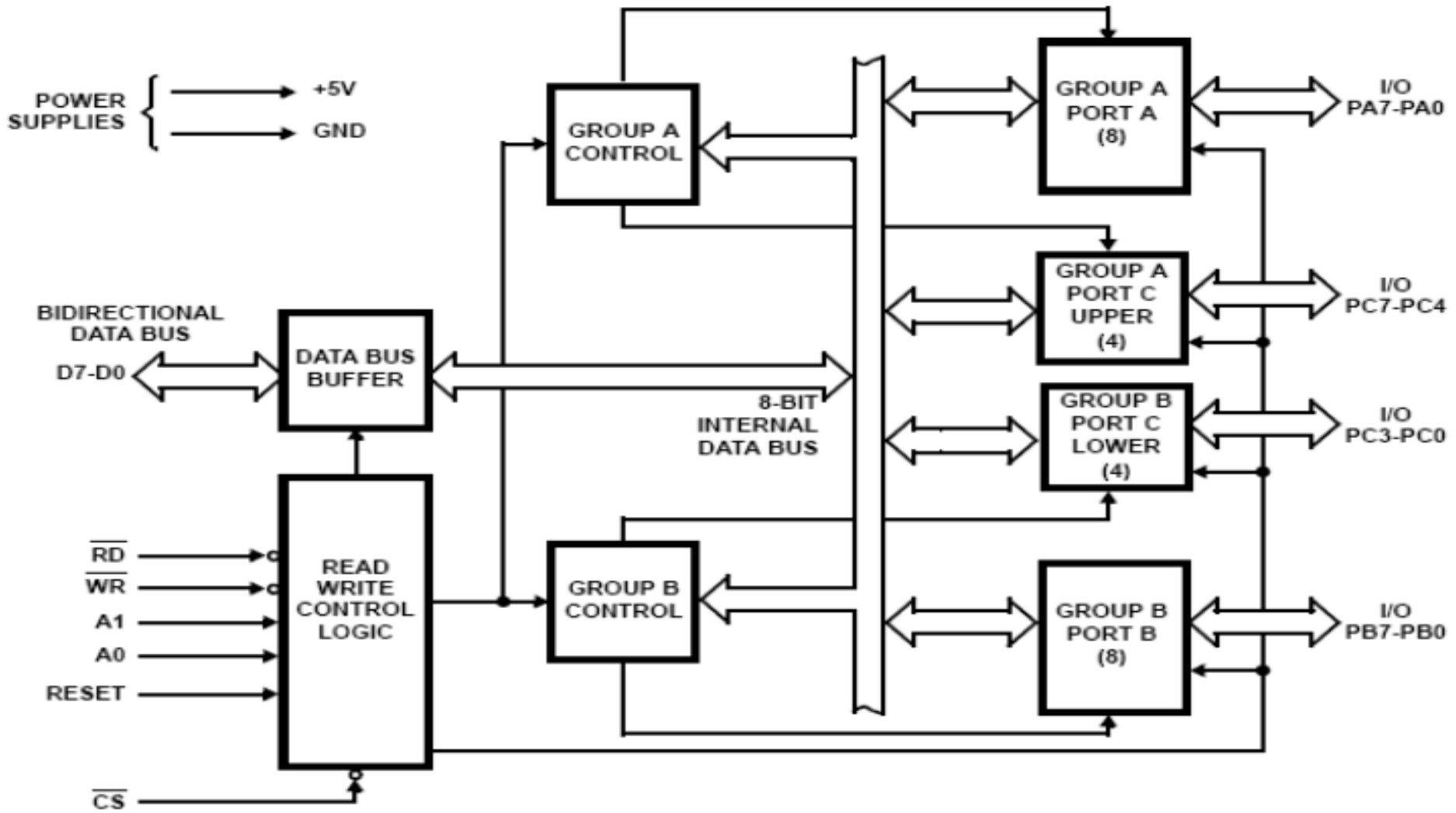
| CS | $A_1$ | $A_0$ | Result           |
|----|-------|-------|------------------|
| 0  | 0     | 0     | PORT A           |
| 0  | 0     | 1     | PORT B           |
| 0  | 1     | 0     | PORT C           |
| 0  | 1     | 1     | Control Register |
| 1  | X     | X     | No Selection     |

# $A_0$ and $A_1$

These input signals work with RD, WR, and one of the control signal. Following is the table showing their various signals with their result.

| $A_1$ | $A_0$ | RD | WR | CS | Result  |
|-------|-------|----|----|----|---|
| 0     | 0     | 0  | 1  | 0  | <b><u>Input Operation</u></b><br>PORT A → Data Bus  |
| 0     | 1     | 0  | 1  | 0  | PORT B → Data Bus                                   |
| 1     | 0     | 0  | 1  | 0  | PORT C → Data Bus                                   |
| 0     | 0     | 1  | 0  | 0  | <b><u>Output Operation</u></b><br>Data Bus → PORT A |
| 0     | 1     | 1  | 0  | 0  | Data Bus → PORT A                                   |
| 1     | 0     | 1  | 0  | 0  | Data Bus → PORT B                                   |
| 1     | 1     | 1  | 0  | 0  | Data Bus → PORT D                                   |

# 8255 BLOCK DIAGRAM



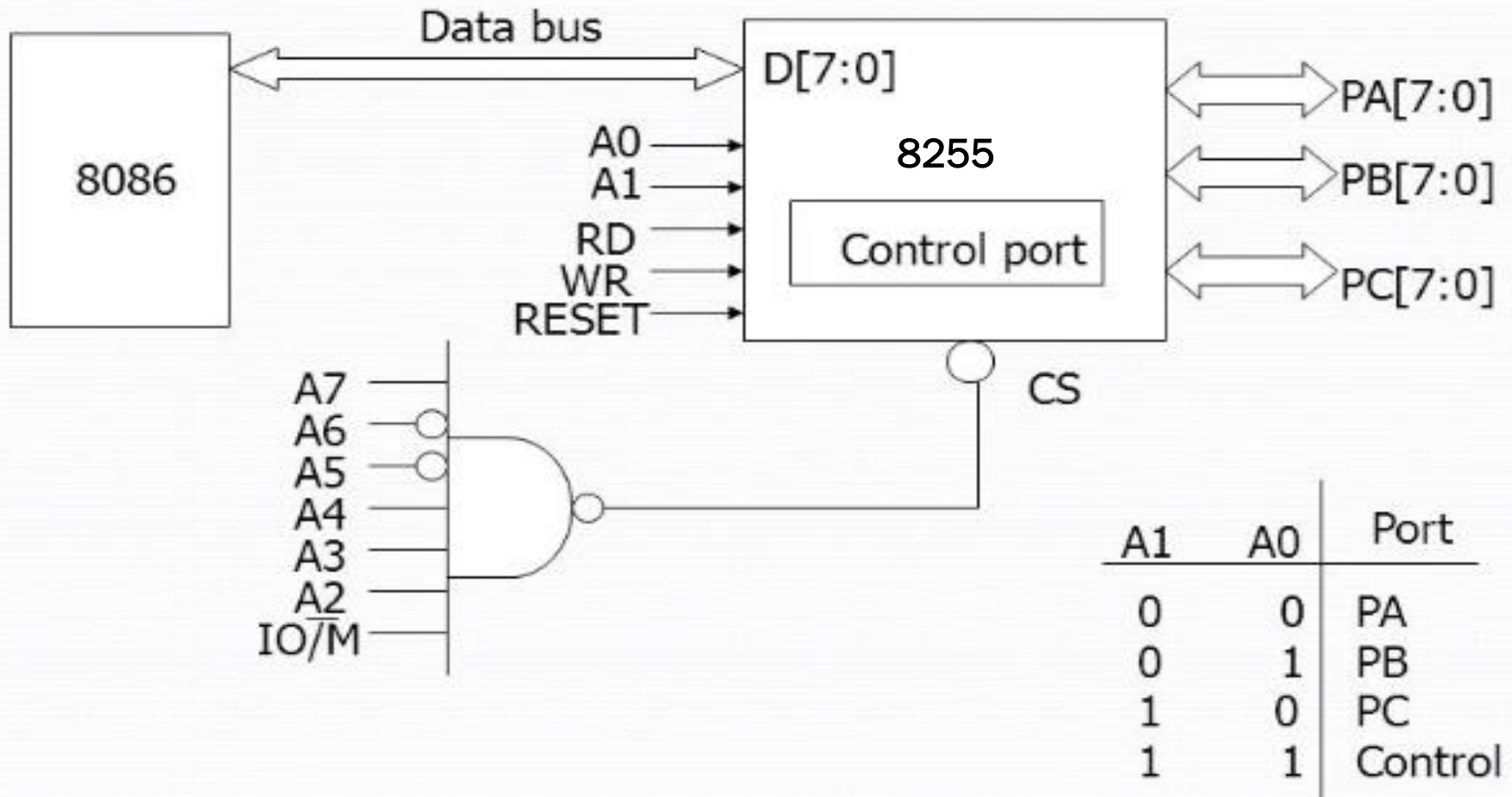
## MODE SELECTION

- operation modes: i) I/O modes (M0,M1,&M2)  
ii) BSR (Bit set/Reset) mode

There are three basic modes of operation that can be selected by control words.

|                                   |                    |
|-----------------------------------|--------------------|
| Mode 0-Basic I/O                  | (Group A, Group B) |
| Mode 1-Strobe input/Strobe output | (Group A, Group B) |
| Mode 2-Two-way bus                | (Port A only)      |

## INTERFACING CIRCUIT OF 8255 AND 8086



## **ADC (ANALOG TO DIGITAL CONVERTER)**

**ADC 0808 is a 28 pin DIP(Dual in line package).**

**It internally has 3:8 analog multiplexer. That means 8 different input can be connected to the chip.**

**Only one of the 8 inputs can be selected for conversion by using 3 address lines .**

## Program:

MOV AL, 98H; Initialize 8255  
OUT CWR, AL;

MOV AL, 02H; Select I/P<sub>2</sub> as analog i/p  
OUT Port B, AL; Port B as o/p

MOV AL, 00H; Give Start of Conversion  
pulse to ADC

OUT Port C, AL;

MOV AL, 01H;

OUT Port C, AL;

MOV AL, 00H;

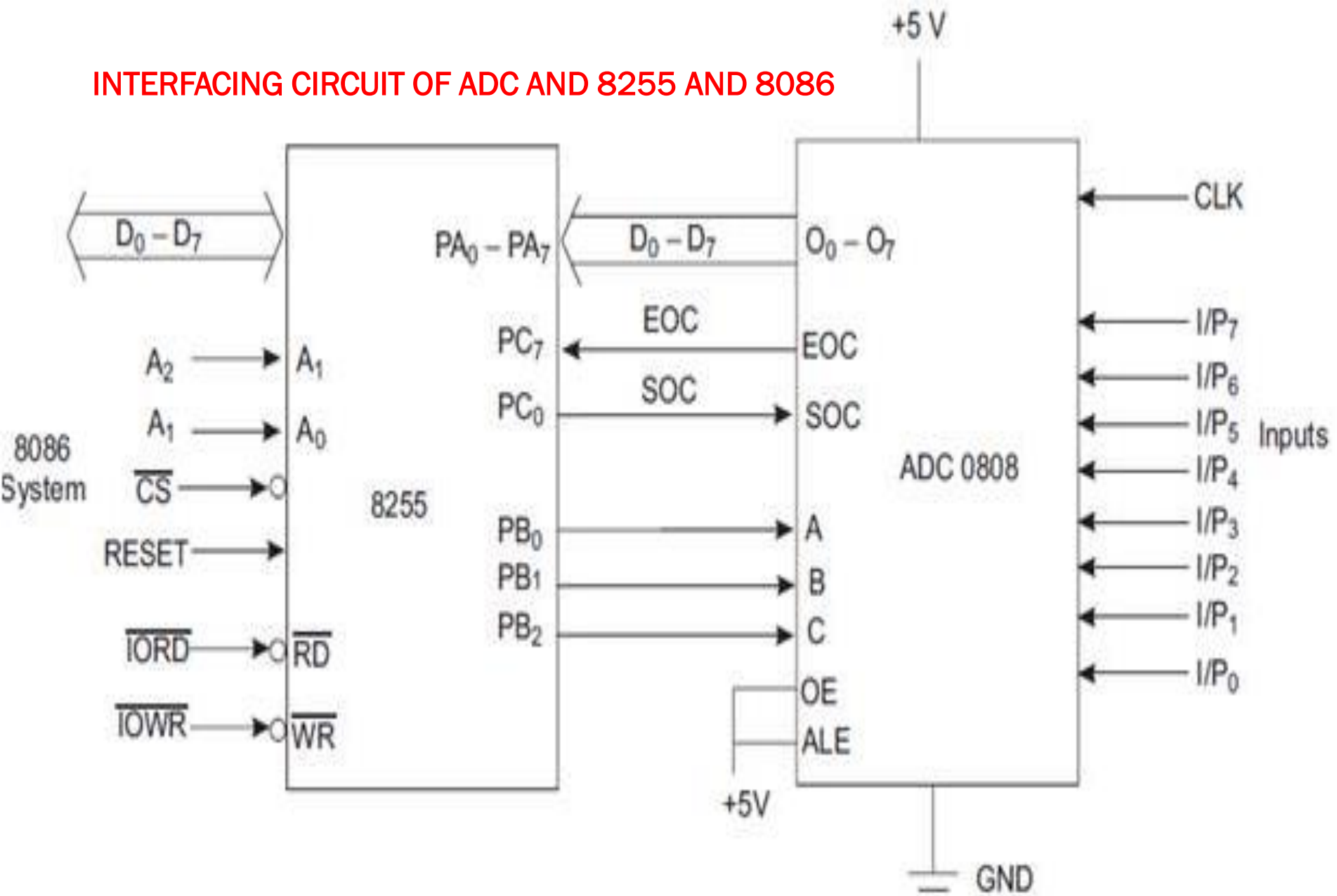
OUT Port C, AL;

WAIT: IN AL, Port C; Check for EOC by  
reading Port C upper  
RCL ; & rotate through carry  
JNC WAIT

IN AL, Port A; if EOC, read digital  
equivalent in AC

HLT; stop

## INTERFACING CIRCUIT OF ADC AND 8255 AND 8086



# Programmable Peripheral Interface

## INTEL-8255

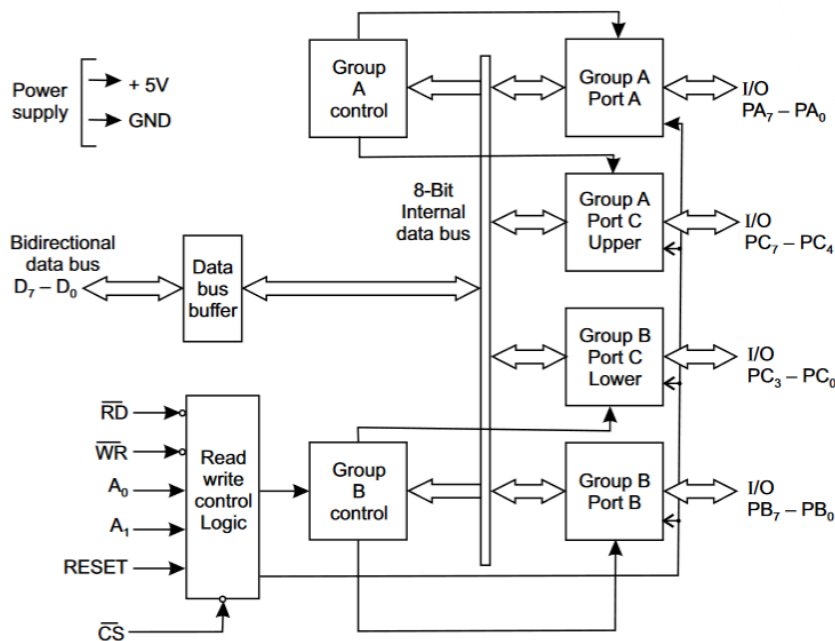
Prepared by: Prof. Md Isteyaque Ashraf  
Guest Faculty, Dep't of ECE  
PCE, Purnea

The 8255 is a general purpose programmable, Parallel I/O device designed for use with Intel microprocessors. It consists of three 8-bit bidirectional I/O ports (24 I/O lines) that can be programmed to transfer data under various conditions from simple I/O to interrupt I/O.

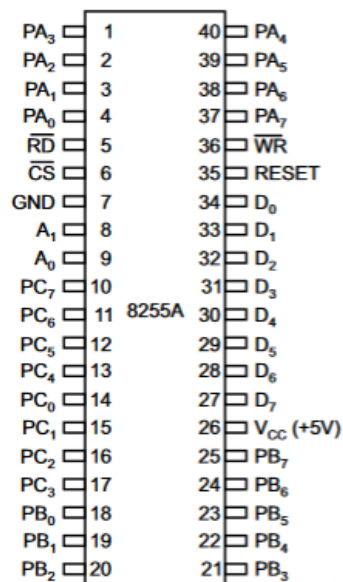
The three ports are PORT A, PORT B & PORT C.

Port A contains one 8-bit output latch/buffer and one 8-bit input buffer. Port B is same as PORT A. However, PORT C can be split into two parts PORT C lower (PC0-PC3) and PORT C upper (PC7-PC4) by the control word. The three ports are divided in two groups Group A (PORT A and upper PORT C) Group B (PORT B and lower PORT C).

### Block Diagram:



### Pin Diagram:



## Read write control logic:

The function of this block is to manage all the internal and external transfers of both data and control or status word. The details of each pin connected with this block are described below.

$\overline{CS}$  (Chip Select)- A “Low” on this input pin enables the communication between the 8085 and MPU.

$A_0$  and  $A_1$ - These are the address lines of 8255 which are directly connected to the MPU lower address lines ( $A_0$ ,  $A_1$ ). The bit combination of these signals are shown below.

| $\overline{CS}$ | $A_1$ | $A_0$ | Selection             |
|-----------------|-------|-------|-----------------------|
| 0               | 0     | 0     | Port A                |
| 0               | 0     | 1     | Port B                |
| 0               | 1     | 0     | Port C                |
| 0               | 1     | 1     | Control Word Register |
| 1               | X     | X     | 8255 is not selected  |

Prepared by: Prof. Md Isteyaque Ashraf  
Guest Faculty, Dep't of ECE  
PCE, Purnea

## PPI 8255 can operate in three modes:

(a) Mode 0 (b) Mode 1 and (c) Mode 2.

Apart from these there is another mode called BSR mode (Bit Set/Reset mode)

The three modes are Mode 0, Mode 1 and Mode 2. These are I/O operations and selected only if D7 bit of the control word register is put as 1. The three operating modes of 8255 are distinguished in the following manner:

Mode 0: This is a basic or simple input/output mode, whose features are:

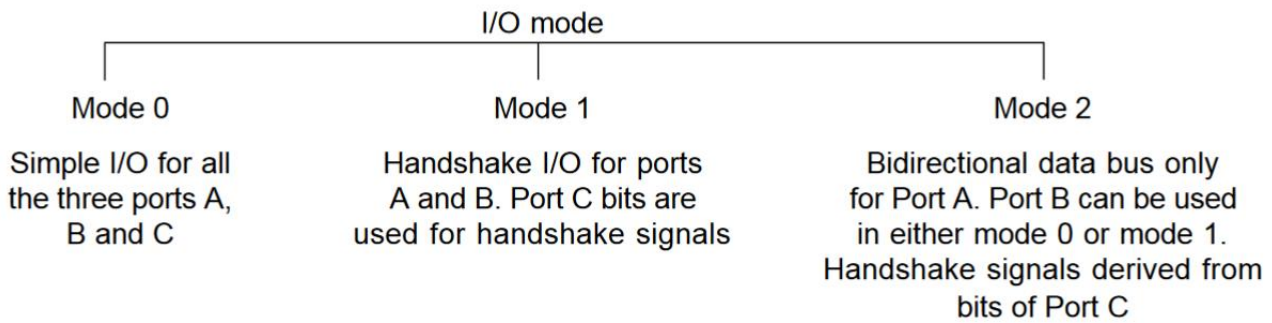
- Outputs are latched.
- Inputs are not latched.
- All ports (A, B,  $C_U$ ,  $C_L$ ) can be programmed in either input or output mode.
- Ports don't have handshake or interrupt capability.
- Sixteen possible input/output configurations are possible.

Mode 1: In this mode, input or outputting of data is carried out by taking the help of handshaking signals, also known as strobe signals. The basic features of this mode are:

- Ports A and B can function as 8-bit I/O ports, taking the help of pins of Port C.
- I/Ps and O/Ps are latched.
- Interrupt logic is supported.
- Handshake signals are exchanged between CPU and peripheral prior to data transfer.
- In this mode, Port C is called status port.
- There are two groups in this mode—group A and group B. They can be configured separately. Each group consists of an 8-bit port and a 4-bit port. This 4-bit port is used for handshaking in each group.

Mode 2: In this mode, Port A can be set up for bidirectional data transfer using handshake signals from Port C. Port B can be set up either in mode 0 or mode 1.

The basic operations of the three modes are shown below:



The control word format, when 8255 is operated in I/O mode, is shown below. For 8255 PPI to be operated in I/O mode, D7 bit must be 1.

The three ports are divided into two groups—Groups A and B. Group A consists of Port A and  $C_U$  ( $PC_4-PC_7$ ). Port A can be operated in any of the modes—0, 1 or 2. Group B consists of Port B and  $C_L$  ( $PC_0-PC_3$ ). Here Port B can be operated in either mode 0 or 1.

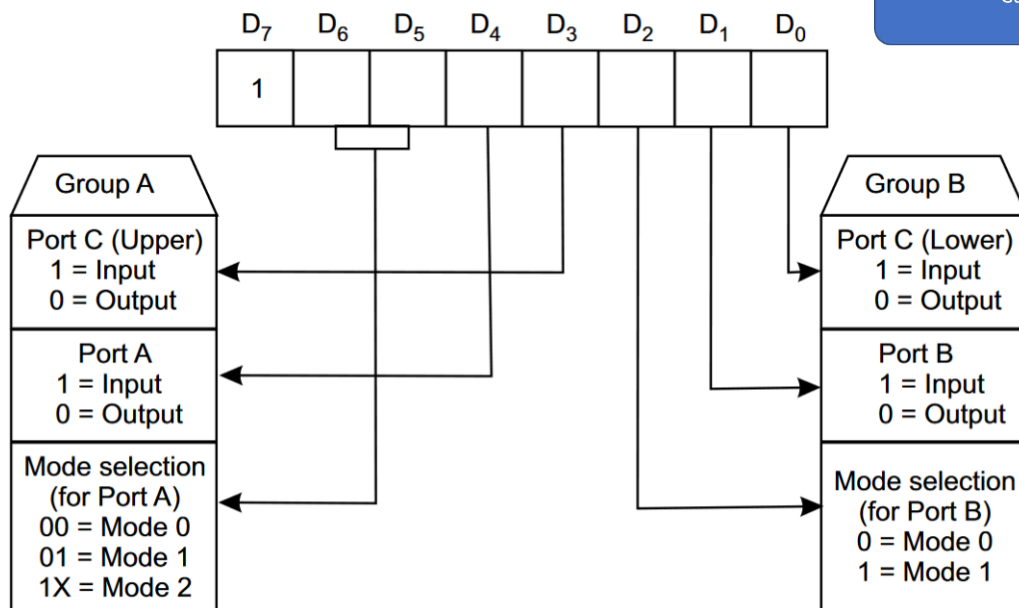


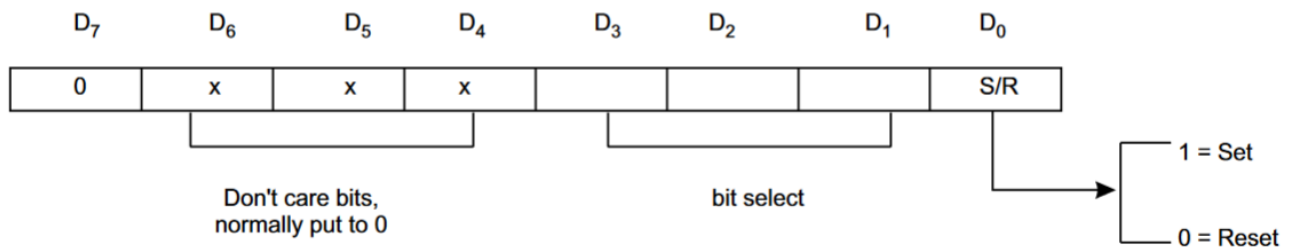
Fig: The CWR in the I/O mode

### BSR (Bit Set Reset mode):

BSR mode stands for Bit Set Reset mode. The characteristics of BSR mode are:

- BSR mode is selected only when  $D_7 = 0$  of the Control Word Register (CWR).
- It is concerned with bits of port C.
- Individual bits of Port C can either be Set or Reset.
- At a time, only a single bit of port C can be Set or Reset.
- Is used for control or on/off switch.
- BSR control word doesn't affect ports A and B functioning.

The content of the control word register will be as follows, when used in the BSR mode and selects (either Sets or Resets) a particular bit of Port C at a time



| $D_3$ | $D_2$ | $D_1$ | Particular bit of Port C selected |
|-------|-------|-------|-----------------------------------|
| 0     | 0     | 0     | Bit 0                             |
| 0     | 0     | 1     | Bit 1                             |
| 0     | 1     | 0     | Bit 2                             |
| 0     | 1     | 1     | Bit 3                             |
| 1     | 0     | 0     | Bit 4                             |
| 1     | 0     | 1     | Bit 5                             |
| 1     | 1     | 0     | Bit 6                             |
| 1     | 1     | 1     | Bit 7                             |

Fig: The CWR in the BSR mode